UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/865,498	05/29/2001	Tetsuo Morita	209174US2	3173

7590 05/05/2004

O9BLON SPIVAK MCCLELLAND MAIER & NEUSTADT
1755 JEFFERSON DAVIS HIGHWAY
FOURTH FLOOR
ARLINGTON, VA 22202

EXAMINER	
KUMAR, SRILAKSHMI K	

ART UNIT	PAPER NUMBER
2675	10

DATE MAILED: 05/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/865,498	MORITA, TETSUO	
	Examiner	Art Unit	
	Srilakshmi K. Kumar	2675	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 February 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *14-21* is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

The following office action is in response to Amendment B, filed February 18, 2004. Claims 1 and 2 have been amended. Claims 1-21 are pending.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura et al (US 6,411,273) in view of Aoki (US 6,011,533).

As to independent claim 1, Nakamura et al disclose a liquid crystal display comprising; a pixel array portion having signal lines and scanning lines horizontally and vertically aligned, and pixel transistors formed in the vicinity of each intersection of said signal line and said scanning line (col. 34, lines 5-8, 13-22); a plurality of first latch circuits configured to latch digital gradation data consisting of a plurality of bits in different timings (Fig. 9, item 102, col. 41, lines 44-col. 42, line 17), said plurality of first latch circuits being provided corresponding to every multiple signal lines (Fig. 9, item 102, col. 41, lines 44-col. 42, line 17); a plurality of second latch circuits which are provided in accordance with each of a plurality of said first latch circuits and latch data latched by each of a plurality of said first latch circuits at the same time (Fig. 9, items 103, col. 41 lines 44-col. 42, line 17); a plurality of D/A converters (Fig. 9, item 104). Nakamura et al do not disclose a signal line selection circuit configured to switch whether said

analog gradation voltage is supplied to each signal line so that said signal lines in said pixel array portion are driven multiple times in units of multiple signal lines. Aoki discloses a signal line selection circuit in Fig. 1, item 102, and col. 8, lines 54-57, col. 15, lines 18-59. It would have been obvious to one of ordinary skill in the art to incorporate the signal line selection circuit into that of Nakamura et al as the signal line selection circuit supplies the signal in a sequence at generated by the timing circuit.

As to dependent claim 2, limitations of claim 1, and further comprising, wherein said signal line selection circuit has a plurality of analog switches, which are provided in accordance with each of said signal lines and switch whether said analog gradation voltage is supplied to corresponding signal line (col. 42, line 51-col. 43, line 24); said signal line selection circuit controls a plurality of said analog switches to be turned on/off so that said signal lines are driven multiple times in units of multiple signal lines (col. 42, line 51-col. 43, line 24).

As to dependent claim 3, limitations of claim 2, and further comprising, wherein said first latch circuits, said second latch circuits, said D/A converters and said analog switches are formed on the same insulating substrate as said signals, said scanning lines and said pixel transistor (col. 34, lines 13-34); a plurality of said analog switches are provided in accordance with each of said D/A converters and a plurality of said analog switches are sequentially turned on one by one (col. 42, line 51-col. 43, line 23).

As to dependent claim 4, limitations of claim 2, and further comprising, wherein the number of signal lines is n (n is an integer not less than 2), n/m sets of said first latch circuits, said second latch circuits and said D/A converters are provided and m pieces of analog switches are provided for each of said D/A converters (Fig. 9, col. 41, lines 44-col. 42, line 17).

As to dependent claim 5, limitations of claim 4, and further comprising, wherein said first latch circuit includes a digital gradation data for said first latch circuit (col. 41, line 44-col. 42, line 17).

As to dependent claim 6, limitations of claim 1, wherein said first latch circuit includes a first level conversion circuit conversion circuit configured to convert digital gradation data into digital gradation data in a first voltage range (col. 41, lines 44-col. 42, lines 17, col. 42, line 51-col. 43, line 23).

As to dependent claim 7, limitations of claim 1, and further comprising, comprising a second level conversion circuit which is inserted between said second latch circuit and said D/A converter (col. 41, lines 8-63).

As to dependent claim 8, limitations of claim 1, and further comprising, wherein said D/A converter includes a decoder configured to decode an output from said second latch circuit (col. 42, line 51-col. 43, line 17); and a plurality of analog switches which are controlled to be turned on/off in accordance with a decoding result by said decoder (col. 42, line 51-col. 43, line 17, col. 45, lines 6-52, col. 46, lines 10-57).

As to dependent claim 9, limitations of claim 1, and further comprising, wherein said D/A converter includes a plurality of resistance devices connected between a first voltage terminal and a second voltage terminal in series (col. 45, lines 6-52, col. 46, lines 10-57).

As to dependent claim 10, limitations of claim 9, and further comprising, a plurality of electric current amplification circuits connected to said respective connection points of a plurality of said resistance devices, wherein selection circuit selects any one of outputs from said

electric current amplification circuits based on an output from said second latch circuit (col. 45, lines 6-52, col. 46, lines 10-57).

As to dependent claim 11, limitations of claim 1, further comprising a shift register configured to output a latch timing signal of each of a plurality of said first latch circuits (Fig. 9, col. 34, lines 5-8, 13-22), wherein a plurality of said second latch circuits carry out the latch operation based on a load signal generated by an output from said shift register (Fig. 9, col. 34, lines 5-8, 13-22).

As to dependent claim 12, limitations of claim 12, limitations of claim 1, and further comprising, wherein said signal line selection circuit selects all signal lines corresponding to either odd numbered pixels or even numbered pixels in a first have of one horizontal line display period, and selects all signal lines corresponding to the other of odd numbered pixels or even numbered pixels in a last half of one horizontal line display period (col. 34, lines 5-55).

As to dependent claim 13, see claim1, above.

Allowable Subject Matter

1. Claims 14-21 are allowed.

2. The following is an examiner's statement of reasons for allowance:

With respect to independent claims 14 and 20, the prior art of record fail to disclose an output circuit having a passing electric current prevention unit which prevents a passing electric current to flow from a power supply terminal of said output terminal to a group terminal in said sampling period.

With respect to dependent claims 15-19 and 21, these claims are allowable as they depend upon an allowed independent claim.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

3. Applicant's arguments filed February 18, 2004 have been fully considered but they are not persuasive.

With respect to applicant's arguments with regards to independent claim 1, Nakamura discloses the latch circuits said plurality of first latch circuits being provided corresponding to every multiple signal lines in Fig. 9, item 102, col. 41, lines 44-col. 42, line 17. Nakamura disclose in col. 41, wherein a liquid crystal display panel is shown where 3 bit data is inputted, and where n pieces of first latch circuits for latching signals. The timing controller (101) successively outputs latch pulses to the first latch circuits according to dot clock signals. A three bit serial signal is thereby latched by each first latch circuit. When the data or one horizontal line is thus latched by each of the first latch circuits, a latch pulse is outputted from the source timing controller to each second latch circuit. Nakamura et al do not disclose a signal line selection circuit configured to switch whether said analog gradation voltage is supplied to each signal line so that said signal lines in said pixel array portion are driven multiple times in units of multiple signal lines. Aoki discloses a signal line selection circuit in Fig. 1, item 102, and col. 8, lines 54-57, col. 15, lines 18-59. It would have been obvious to one of ordinary skill in the art to incorporate the signal line selection circuit into that of Nakamura et al as the signal line selection

circuit supplies the signal in a sequence at generated by the timing circuit. Thus the rejection above is maintained.

Conclusion

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Srilakshmi K. Kumar whose telephone number is 703 306 5575. The examiner can normally be reached on 8:00 am to 4:30 pm.

The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Srilakshmi K. Kumar
Examiner
Art Unit 2675

SKK
May 2, 2004

DENNIS-DOON CHOW
PRIMARY EXAMINER